

FIG.1

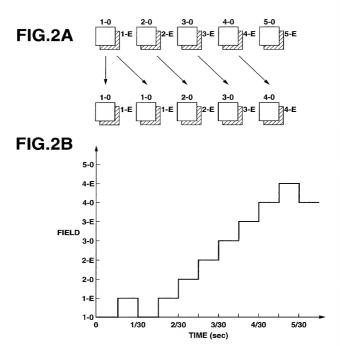




FIG.3A

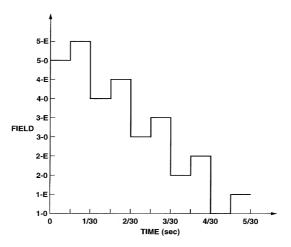


FIG.3B

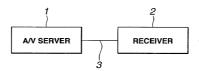


FIG.4

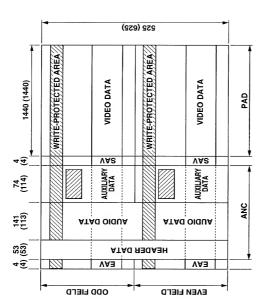


FIG.5

0										10	11 26	27	42	43									5
ADF	ADF	ADF	QIQ	SDID	Data count	Line No.0	Line No.1	Line No.CRC 0	Line No.CRC 1	CODE&AAI	Destination address	Source address		Block type	CRC flag	Data extend flag	Reserved 0	Reserved 1	Reserved 2	Reserved 3	Header CRC 0	Header CRC 1	

FIG.6

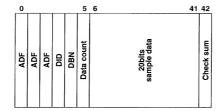


FIG.7A

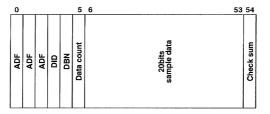


FIG.7B

0	_	_	г	_			_	8	9				14	15	16	17	1
ADF	ADF	ADF	QIQ	alas	Data count	AF (UDW0)	RATE (UDW1)	ACT (UDW2)			DEL m-m (UDW 3-8)			à	(UDW 9-10)	Check sum	

FIG.8

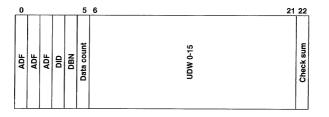


FIG.9

_0					5	3		21	22	
ADE	ADF	ADF	QIQ	DBN	Data count		UDW 0-15		Check sum	

FIG.10

0						7	8	21 2	22
ADF	ADF	ADF	DBN	Data count	Activeline (UWD0)	Slowcontrol (UWD1)	UDW 2-15		Check sum

**FIG.11** 

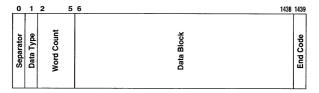
BIT	
7	Reserved
6	Reserved
5	Reserved
4	Contents information
3	Combination of
2	the memory address
1	
0	

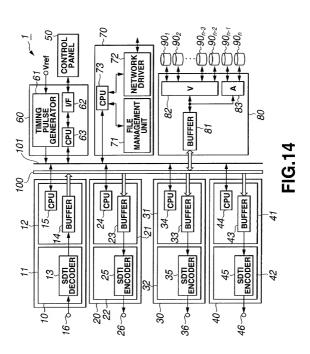
**FIG.12** 

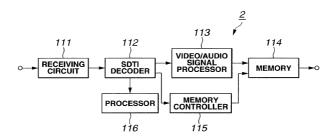




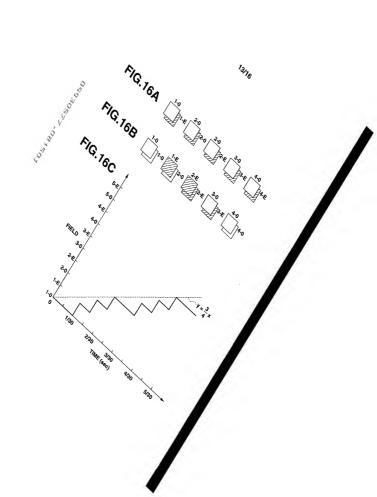
## FIG.13B

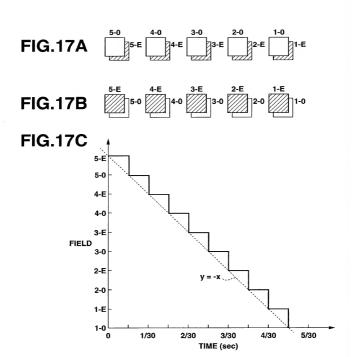


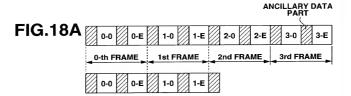




**FIG.15** 







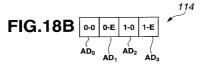
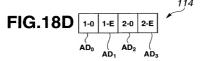


FIG.18C 1-0 1-E



30 2-0 2-E 2-0 2-E 2-0 2-E ADo AD1 AD2 AD3 Ah 2-0 2-E 114 - 1-0 1-E 2-8 2-E ADo AD1 AD2 AD3 Fh 1-0 1-E 1-0 1-E 1-0 | 1-E | 1-0 | 4-E ADo AD1 AD2 AD3 Bh 1-0 1-E 11-8 14-E 0-0 0-E 1-0 1-E AD<sub>0</sub> AD<sub>1</sub> AD<sub>2</sub> AD<sub>3</sub> 6 10 01 AĎ<sub>0</sub> ÁĎ<sub>1</sub> ÁĎ<sub>2</sub> ÁĎ<sub>3</sub> Bh 9-0-0 0-0 9-0 0-0 B-0 0-0 AD<sub>0</sub> AD<sub>1</sub> AD<sub>2</sub> AD<sub>3</sub> Ah 0-0 O-E 0-0 0-E 0-0 0-E FIG.19A

FIG.19B

(AD<sub>2</sub>) (AD<sub>2</sub>) (AD<sub>2</sub>) (AD<sub>3</sub>) (AD<sub>1</sub>) (AD<sub>2</sub>) (AD<sub>3</sub>) (AD<sub>3</sub>

AD<sub>0</sub> AD<sub>1</sub> AD<sub>2</sub> AD<sub>3</sub>

TIME